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# High-Performance Quasi-Z-Source Series Resonant DC–DC Converter for Photovoltaic Module-Level Power Electronics Applications

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***Abstract*—This paper presents the high-performance quasi-Z-source series resonant dc–dc converter as a candidate topology for the photovoltaic module-level power electronics applications. The converter features a wide input voltage and load regulation range thanks to the multimode operation, i.e., when the shoot-through pulse width modulation and phase-shift modulation are combined in a single switching stage to realize the boost and buck operating modes, respectively. Our experiments confirmed that the proposed converter is capable of ensuring ripple-free 400 V output voltage within the sixfold variation of the input voltage (from 10 to 60 V). The converter prototype assembled achieved a maximum efficiency of 97.4%, which includes the auxiliary power and control system losses.**

***Index Terms*—DC–DC converter, module-level power electronics (MLPE), module-integrated converter, quasi-Z-source (qZS) converter, renewable energy, resonant converter, solar photovoltaic (PV).**

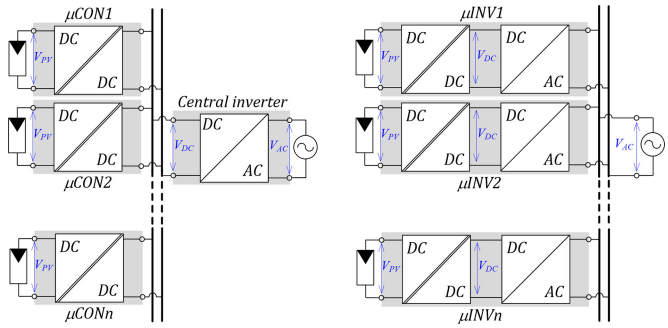


Fig. 1. Full-power converters for the parallel connection of PV modules: microconverters ($\mu CON$) with (a) common dc bus and microinverters ($\mu INV$) with (b) grid-side connection.

## I. Introduction

MODULE-LEVEL power electronics (MLPE) is a topic of growing interest in the solar photovoltaic (PV) applications. The idea of MLPE is to allow operation of each PV module in the maximum power point (MPP) and, therefore, to ensure the best possible energy harvest. Generally, the MLPE concepts could be classified as the full-power and partial-power processing converters [1]. The full-power MLPE concepts could be categorized as those connecting PV panels in series and in parallel. The first group is mostly represented by the PV power optimizers, which are typically realized with the nonisolated boost [2] and buck–boost converters [1]. The main focus of this paper is on the full-power converters for the parallel connection of PV modules. In this approach, each PV panel is equipped with a microconverter ($\mu CON$) with outputs connected in parallel to the central dc bus of the PV power system [see Fig. 1(a)]. $\mu CON$ is a self-powered high-efficiency step-up dc–dc converter with galvanic isolation that operates with autonomous control and is integrated to the PV panel for tracking the MPP locally. The galvanic isolation is essential to reduce ground leakage currents and grid current total harmonic distortion [3]. As seen from Fig. 1(a), the central inverter feeds PV power to the grid.

The microinverter ($\mu INV$) concept presented in Fig. 1(b) allows parallel connection of PV modules at the grid side [4]. In that case, each PV module features direct ac connectivity since $\mu INV$ integrates both the galvanically isolated step-up dc–dc converter and the grid-tied inverter. This concept is common now in residential and small commercial PV power systems mostly because of its expandability as well as simplicity of installation and maintenance.

Both of the approaches discussed (see Fig. 1) usually require the dc–dc converter, which must ensure high step-up ratio of the input voltage, maximum power point tracking (MPPT), at the same time, providing high conversion efficiency. To analyze the technology trends in this field, the state-of-the-art galvanically isolated step-up dc–dc converter topologies for MLPE applications are discussed in Section II. Section III proposes the novel galvanically isolated series resonant quasi-Z-source (qZS) dc–dc converter as a candidate topology for MLPE applications. Section IV analyzes the multimode operation principle of the

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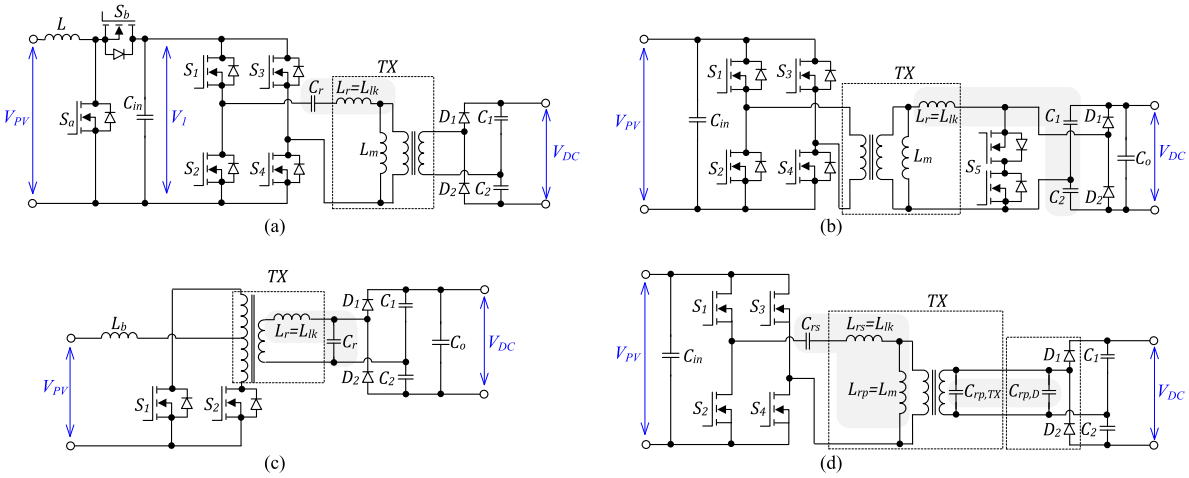


Fig. 2. State-of-the-art dc–dc converters for MLPE applications: (a) double-stage topology combined from a front-end synchronous boost converter and SRC, (b) double-stage topology combined from a SRC and a back-end boost converter based on the bidirectional ac switch, (c) single-stage approach based on the parallel resonant current-fed push–pull converter, and (d) single-stage multiresonant converter.

proposed converter. Further, Sections V and VI present the selected design guidelines and analysis of experimental results. Finally, conclusions are drawn in Section VII.

## II. Recent Advances in Galvanically Isolated DC–DC Converters for MLPE Applications

For the last 20 years, the MLPE application was an object of increased research interest all over the world. An insight to the MLPE technology trends is given in several review papers [1], [5]–[7]. Except the efficiency, power density, reliability, and price per watt issues, one of the recent challenges in the design of a good MLPE system is a wide input voltage regulation range. A high-efficiency dc–dc converter with extended input voltage regulation range will support the implementation of the global MPP tracking algorithms, which can substantially improve the energy yield from the PV module under the partial shading conditions [8]. The majority of commercial microinverters today feature the minimum level of the MPP voltage in the range from 22 V [9] to 27 V [10]. To feed power to the grid in European conditions, the grid-side dc-link voltage should be around 400 V; therefore, the maximum dc voltage gain of these converters ($G{=}V_{DC}/V_{PV}$ according to Fig. 1) lies in the range from 14.8 to 18.2. A further decrease of the MPP voltage, for example, to 10 V, could bring the performance level of the microinverters to that of the PV power optimizers [11]. Next, emerging topologies of the high step-up galvanically isolated dc–dc converters for MLPE applications are discussed.

Generally, the high step-up galvanically isolated dc–dc converters for MLPE applications can be categorized as those with a double stage or with a single stage power conversion. In the first case, the front-end boost converter preregulates the varying voltage of the PV module to a certain constant voltage level so that the input inverter stage of the high step-up dc–dc converter operates with a near-constant duty cycle. To enhance the efficiency of the double stage conversion approach, the combination of a synchronous boost converter with a series resonant dc–dc converter was proposed in [12]. Such a combination [see Fig. 2(a)] resulted in the efficiency close to 97% at a power level of 200 W and it features a wide input voltage regulation range from 15 to 45 V. Another approach called hybrid series resonant and pulse width modulation (PWM) boost converter [13] contains a combination of a full-bridge series resonant dc–dc converter with a back-end boost converter based on the bidirectional ac switch [see Fig. 2(b)]. Thanks to its hybrid structure, the converter is able to regulate the input voltage in a range from 15 to 55 V by using the simple fixed-frequency PWM control and maintaining relatively high efficiency over the entire input voltage and load regulation range.

In a single-stage dc–dc power conversion, the primary inverter should operate within a wide input voltage range and optimization of the efficiency could become an issue. Here, different approaches were developed to achieve better performance. The simplest structure based on two interleaved flyback converters was proposed by Enphase Energy [14] and due to its overall simplicity, could still be referred to as one of the most popular power conversion approaches for MLPE systems. However, due to its single-ended nature, the main disadvantages of the flyback topology are poor utilization of the isolation transformer and a need for active clamp circuits to minimize the voltage stress of the main switches in the conditions of wide input voltage and load regulation.

To enhance the performance of a single-stage dc–dc power conversion approach, it seems more feasible to implement double-ended topologies such as full-bridge, half-bridge or push–pull. For example, the soft-switching current-fed push–pull converter proposed in [15] [see Fig. 2(c)] comprises only two switches and allows the nonisolated gate drivers to be used. Thanks to the parallel resonance between the leakage inductance of the isolation transformer and the resonant capacitor $C_r$, the transistors are turned on and off at the zero-voltage and zero-current conditions. The diodes of the voltage doubler rectifier (VDR) are also turned off at the zero current, which finally results in a peak efficiency of 96.6% and input voltage regulation range of 20 to 40 V.

Another original approach to the single-stage dc–dc power conversion for MLPE applications was discussed in [16]. The proposed multiresonant full-bridge dc–dc converter

TABLE I
PERFORMANCE COMPARISON OF NEW EMERGED HIGH STEP-UP DC–DC CONVERTERS FOR MLPE APPLICATIONS

| Fig. [ref] | $P_{max}$ (W) | $V_{PV}$ (V) | $V_{DC}$ (V) | Peak eff. (%) | Type of resonance |
|---|---|---|---|---|---|
| 2a [12] | 275 | 15–45 | 400 | 97 | Series |
| 2b [13] | 300 | 15–55 | 320 | 97.4 | Series |
| 2c [15] | 244 | 20–35 | 700 | 96 | Parallel |
| 2d [16] | 250 | 20–40 | 400 | 96.6 | LLCC |

[see Fig. 2(d)] features the series and parallel resonant tanks formed by the leakage and magnetizing inductances of the isolation transformer, respectively. The parallel capacitance $C_P$ is a sum of the parasitic capacitances of the rectifying diodes $C_{rp,D}$ and the isolation transformer $C_{rp,TX}$. In this topology, the resonant tank optimized carefully leads to a peak efficiency of 96% and the input voltage range from 20 to 35 V. To regulate the input voltage, the frequency control is used and the switching frequency is changed in a range from 215 to 268.5 kHz.

The performance of the state-of-the-art dc–dc converter topologies for MLPE applications is compared in Table I. As can be seen, the "best-in-class" converters feature a three- to almost fourfold input voltage regulation range with the peak efficiency of 97%. Further, generalizations regarding the technology development trends in the MLPE systems could be as follows.

1) Resonant power conversion is an important attribute of the modern galvanically isolated dc–dc converters for PV applications since it allows the soft switching of semiconductors and could help to improve the power density of the converter by increasing the switching frequency. The most popular type of resonance used is the series resonance with the maximum possible utilization of the parasitic elements of the circuit, i.e., leakage inductance of the transformer.
2) VDR is typically used in the secondary side of the converter to reach higher dc voltage gain at a given transformer turns ratio. Furthermore, the VDR enables realization of the integrated series resonant tank at the secondary side of the converter, i.e., when the leakage inductance of the isolation transformer is used as a resonant inductor and capacitors of the VDR are used as resonant capacitors.
3) Implementation of the wide-bandgap semiconductors enables the peak efficiencies to be well over 97%. It seems to be most feasible to use SiC Schottky barrier diodes (SBD) in the VDR with the output voltages over 380 VDC since they feature extremely low reverse recovery charge, which results in the low switching losses and higher efficiency. Moreover, the high operating junction temperature of the SiC SBD is especially important in terms of the high thermal stress and reliability requirements applied to the MLPE systems. To improve the efficiency further, GaN transistors could be implemented; however, it could also impose some cost penalties, especially in the current situation when the per watt prices of the MLPE systems are ramped down.

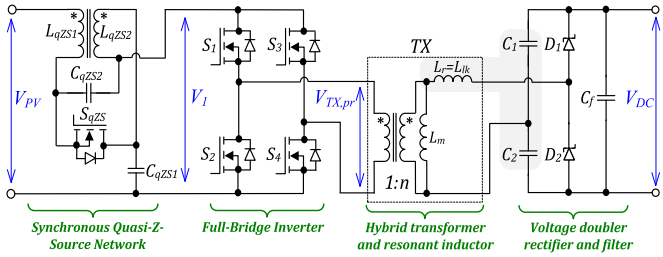


Fig. 3. Generalized topology of the galvanically isolated qZSSRC.

## III. GALVANICALLY ISOLATED QUASI-Z-SOURCE SERIES RESONANT DC–DC CONVERTER (QZSSRC)

In this paper, the galvanically isolated qZSSRC is examined as a candidate topology for PV MLPE applications (see Fig. 3). The converter consists of the qZS network ($L_{qZS1}$, $L_{qZS2}$, $C_{qZS1}$, $C_{qZS2}$, $S_{qZS}$), a full-bridge inverter ($S_1$–$S_4$), a step-up isolation transformer *TX*, and the VDR ($D_1$, $D_2$, $C_1$, $C_2$). At its secondary side, the converter has a series resonant tank formed by the leakage inductance of the isolation transformer and the VDR capacitors. The output filter capacitance $C_f$ is used for the output voltage filtering as well as to buffer the double line frequency voltage ripple caused by a grid-side inverter.

To improve the performance, a number of modifications were introduced to the baseline qZSSRC topology, which was originally proposed in [17]. First, to reduce the conduction losses in the input stage of the converter, the concept of the synchronous qZS network was implemented [18], [19]. In the original qZS network [20], a diode is needed to avoid short-circuiting of the capacitors $C_{qZS1}$ and $C_{qZS2}$ during the shoot-through states. In the synchronous qZS network (see Fig. 3), the *n*-channel MOSFET $S_{qZS}$ is placed instead of the diode and is synchronized with the inverter switches such that it conducts only during the active states of the inverter. To prevent conduction of the $S_{qZS}$ during the shoot-through states, a dead-time is introduced before its turn on and off transients.

Another important modification of the qZS network is the implementation of a coupled inductor instead of two discrete inductors in the traditional approach [20]. This modification resulted in both higher power density of the converter and an extra benefit from using the input (PV side) wiring inductance for further reduction of the input current ripple of the converter. The qZSSRC topology proposed combines numerous advantages of the voltage-fed and current-fed converters, while utilizing the best practice of the full-bridge impedance-source converter implementation [21].

As compared to the baseline qZSSRC topology, the proposed converter contains the fully integrated series resonant tank at the secondary side (secondary resonance). On one hand, the capacitors of the VDR, which are charged and discharged in parallel, form the resonance capacitor with an equivalent capacitance value $C_r$:

$$C_r = C_1 + C_2 \tag{1}$$

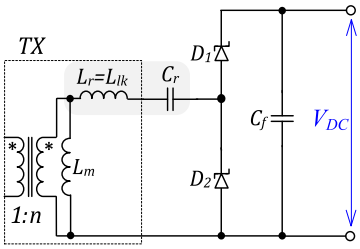


Fig. 4. Greinacher VDR as an alternative option for the qZSSRC secondary side.

where $C_1$ and $C_2$ are the capacitance values of VDR capacitors. On the other hand, the series resonant tank is formed by the leakage inductance of the isolation transformer referred to the secondary winding ($L_{lk}$); therefore, the resonant frequency can be defined as follows:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_{lk}\cdot C_r}} = \frac{1}{2\pi}\sqrt{\frac{1}{L_{lk}\cdot (C_1+C_2)}}. \quad (2)$$

It should be noted that the second resonance frequency also exists due to the magnetic integration of the resonant inductor:

$$f_{r2} = \frac{1}{2\pi}\sqrt{\frac{1}{(L_{lk}+L_m)\cdot C_r}} \quad (3)$$

where $L_m$ is the magnetizing inductance of the isolation transformer referred to the secondary winding. Typically, the leakage inductance of the transformer is below 2 % of the value of the magnetizing inductance [12] and the resonance frequencies $f_r$ and $f_{r2}$ differ by a factor of 10.

The integrated resonant tank implemented enables avoiding the size and cost penalties associated with the use of external resonant elements. The secondary side of the proposed converter could be further simplified by the implementation of the Greinacher VDR (see Fig. 4). In that case, the first capacitor of the VDR acts as a resonant capacitor $C_r$ and the second operates as a buffer of the double line voltage ripple from the grid-side inverter. However, in this VDR configuration, the capacitors have different voltage stresses. In addition, the current stresses are also different since their capacitance values differ by more than ten times, which is caused by their different functions.

## IV. Multimode Operating Principle of the qZSSRC

To extend the input voltage regulation range without serious efficiency penalties, the proposed module-integrated converter uses a multimode operation. Due to the unique properties of the qZS network, the qZSSRC is capable of combining the shoot-through PWM and ordinary phase-shift modulation (PSM) for the realization of the boost and buck operating modes, respectively. Moreover, in the boundary between these modes, the converter operates in a normal mode as a pure series resonant converter (SRC) at the resonant frequency. Fig. 5 shows an example of idealized control variables of the proposed qZSSRC operating within the input voltage range from $0.5{\cdot}V_{PV(MPP)}$ to $1.5{\cdot}V_{PV(MPP)}$. Next, the operating principle of the converter in these three modes is analyzed in detail.

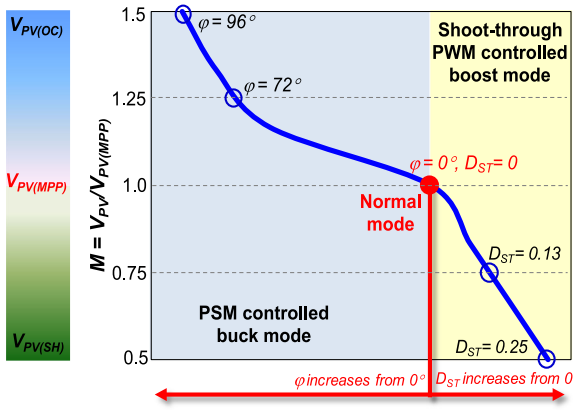


Fig. 5. Example of operating modes and idealized control variables of the multimode qZSSRC.

In order to simplify the analysis of the operating modes of the converter, the following assumptions were made:

1) the converter features no power dissipation in the elements;
2) MOSFET switches are ideal except for their body diodes and OUTPUT capacitances;
3) output filtering capacitance $C_f$ is large enough so that the dc output voltage $V_{DC}$ can be considered as ripple free;
4) the transformer is composed of an ideal transformer with turns ratio 1:$n$, a magnetizing inductance $L_m$, and a leakage inductance $L_{lk}$, both referred to the secondary winding;
5) $C_f$ is much larger than the VDR capacitors $C_1$ and $C_2$, and, therefore, has no influence on the resonance process;
6) VDR capacitors $C_1$ and $C_2$ have equal capacitance values and their sum is represented as $C_r$.

### A. Normal Mode

According to Fig. 5, the normal mode corresponds to the MPP of the PV module at the most common operating conditions. In this operating point, the duty cycle of the inverter switches is close to 0.5 after the dead-time deduction. The switch $S_{qZS}$ is constantly conducting and the operation of the qZSSCR is similar to that of the traditional SRC operating at the resonant frequency. The steady-state waveforms of the qZSSRC operating in the normal mode are presented in Fig. 6.

Next, the operation principle of the qZSSRC in the normal mode is analyzed for the positive half-cycle:

[$t_0$<$t$<$t_1$, Fig. 8(a)]: switches $S_1$ and $S_4$ are turned on and input voltage $V_{PV}$ is applied to the primary winding of the isolation transformer. Since the switching frequency is equal to the resonant frequency ($f_{SW} = f_r$), the current of the $L_{lk}$ and the voltage of the parallel combination of $C_1$ and $C_2$ fully resonate, which results in almost pure sinusoidal waveforms. The current of the magnetizing inductance $L_m$ linearly increases to its maximum value

$$i_{Lm(p)} = \frac{V_{PV}\cdot n\cdot T_{SW}}{4\cdot L_m}. \quad (4)$$

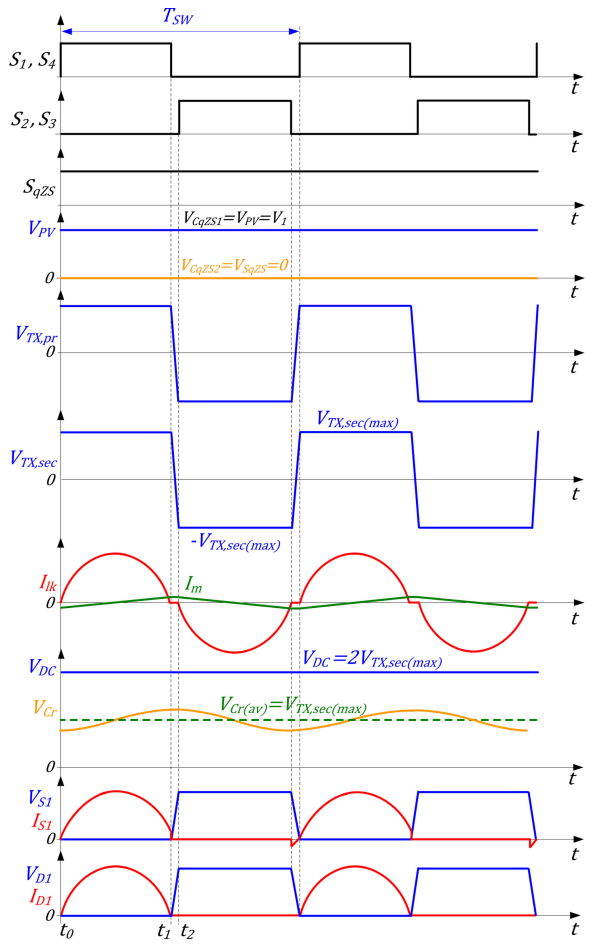


Fig. 6. Steady-state waveforms of the qZSSRC operating in the normal mode.

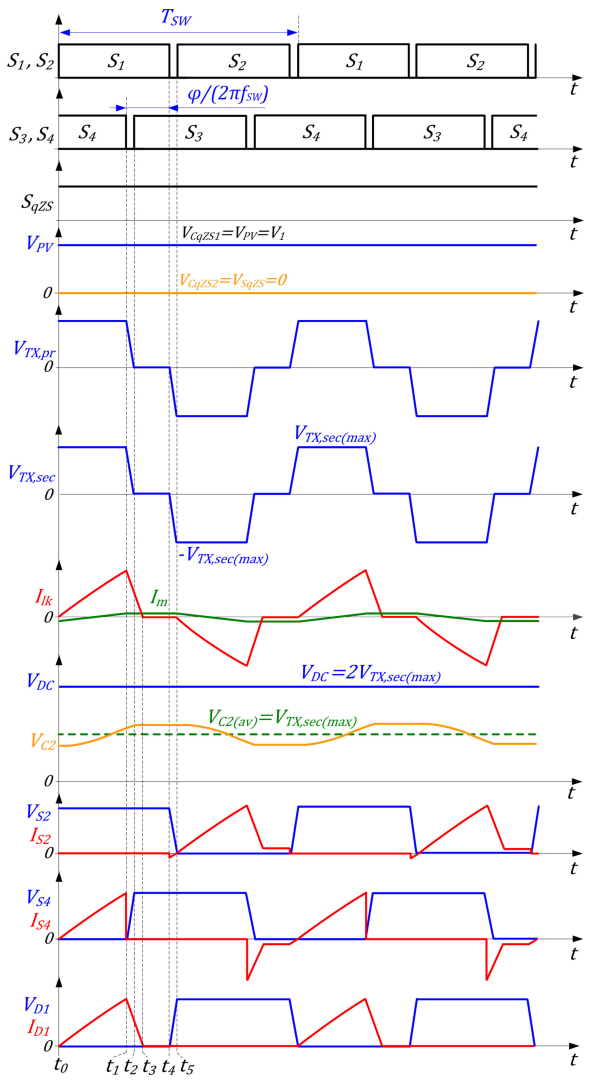


Fig. 7. Steady-state waveforms of the qZSSRC operating in the buck mode.

The switching frequency is equal to the resonant frequency. As a result, at the instant $t_1$, the resonant current reaches zero, and the switches $S_1$ and $S_4$ as well as the VDR diode $D_1$ turn off at zero current. The magnetizing current, which is still present in the switches $S_1$ and $S_4$, could be considered as relatively small; therefore, it is assumed that $S_1$ and $S_4$ are also commutated in the near zero-current switching (ZCS) conditions.

[$t_1<t<t_2$, Fig. 8 (b)]: switches $S_1$ and $S_4$ are turned off and the qZSSRC features dead-time of the inverter during this time interval. The magnetizing inductance of the isolation transformer charges the output capacitances of $S_1$ and $S_4$ and, at the same time, discharges the output capacitances of $S_2$ and $S_3$. If the dead-time and magnetizing inductance of the isolation transformer are correctly dimensioned, the drain-source voltages of $S_2$ and $S_3$ will reach zero before the beginning of the next resonance half-cycle. Therefore, it could be stated that at $t_2$, the switches $S_2$ and $S_3$ will be turned on under the zero-voltage switching (ZVS) conditions. In practice, the minimum dead-time required depends on the operating point and ambient temperature. Hence, it has to be selected large enough in order to discharge capacitors to zero voltage, or even force corresponding body diodes to the conduction state before the instant $t_2$, as shown in Fig. 8 (c), regardless of the operating point.

In the normal mode, the average voltage of the qZS capacitors can be calculated using a volt–second balance of the qZS inductors in the steady state, considering that the connection of the qZS network components

$$\begin{cases} V_{CqZS1(\text{normal})}=\int_0^{T_{SW}} v_{CqZS1}(t)dt=V_{PV}-\int_0^{T_{SW}} v_{LqZS1}(t)dt=V_{PV} \\ V_{CqZS2(\text{normal})}=\int_0^{T_{SW}} v_{CqZS2}(t)dt=-\int_0^{T_{SW}} v_{LqZS2}(t)dt=0 \end{cases} \tag{5}$$

where $V_{CqZS1}$ and $v_{CqZS1}(\mathrm{t})$ are the average and instantaneous voltages of the capacitor $C_{qZS1}$, respectively; $V_{CqZS2}$ and $v_{CqZS2}(\mathrm{t})$ are the average and instantaneous voltages of the capacitor $C_{qZS2}$, respectively; $v_{LqZS1}(\mathrm{t})$ and $v_{LqZS1}(\mathrm{t})$ are the instantaneous voltages of the qZS network inductors $L_{qZS1}$ and $L_{qZS2}$, respectively.

The average voltage of the VDR capacitors is half the output voltage and their voltage ripple could be found as follows:

$$\Delta v_{Cr(\text{normal})} = \frac{P \cdot T_{SW}}{4 \cdot V_{DC} \cdot C_r} \tag{6}$$

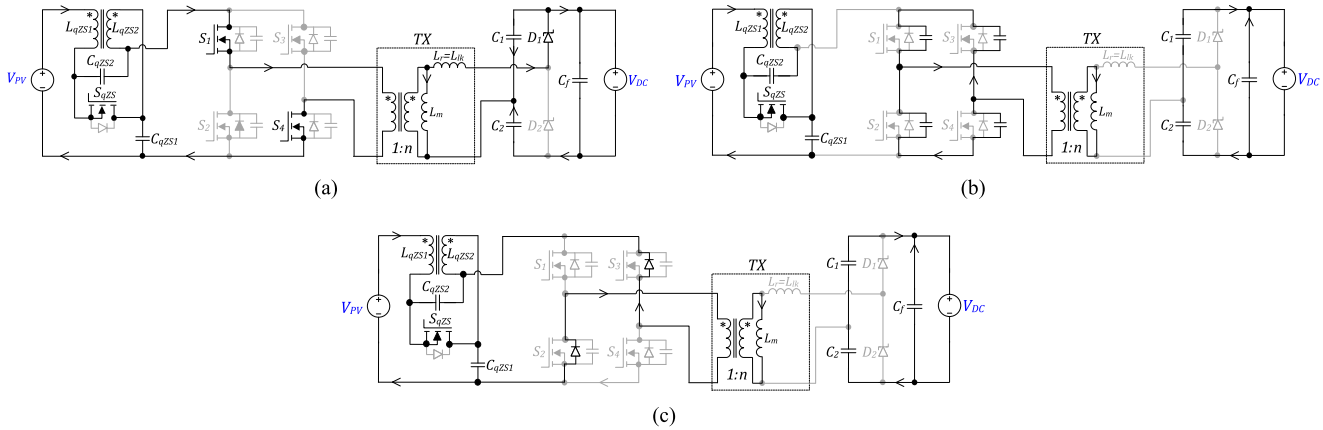


Fig. 8. Generalized equivalent circuits of the qZSSRC operating in the normal mode: (a) $t_0<t<t_1$, (b) $t_1<t<t_2$, and (c) directly before instant $t_2$.

where $P$ is the operating power of the converter. The normalized voltage gain of the qZSSRC in the normal mode could be expressed by (7) and is similar to that of the traditional SRC operating at the resonant frequency

$$G_{\text{normal}} = \frac{V_{DC}}{2 \cdot n \cdot V_{PV}} = 1. \tag{7}$$

### *B. Buck Mode*

When the input voltage is higher than the predefined nominal value, the converter starts to operate in the buck mode. In this case, the qZSSRC could be regarded as a SRC operating in the buck mode when the output voltage is controlled by the PSM at the resonant frequency. As a result, the phase-shift angle $\varphi$ between the two inverter legs and the quality factor ($Q$) at the resonant frequency ($f_{SW}=f_r$) define the dc voltage gain. Fig. 7 shows the steady-state waveforms of the converter in the buck mode.

[$t_0<t<t_1$, Fig. 9(a)]: switches $S_1$ and $S_4$ are turned on and input voltage $V_{PV}$ is applied to the primary winding of the isolation transformer. The current of the $L_{lk}$ and the voltage of the parallel combination of $C_1$ and $C_2$ start to resonate and the magnetizing current linearly increases to its maximum value:

$$i_{Lm(p)} = \frac{V_{PV} \cdot n \cdot T_{SW}}{2 \cdot L_m} \times \frac{\phi}{360}. \tag{8}$$

[$t_1<t<t_2$, Fig. 9(b)]: at $t_1$, the switch $S_4$ turns off with ZVS and the converter enters the dead-time interval. Since the resonance was suddenly interrupted, the currents are still present in the leakage and magnetizing inductances of the isolation transformer. They discharge the output capacitance of $S_3$ while charging the output capacitance of $S_4$. This will ensure the ZVS turn-on of $S_3$ at the instant $t_2$. Its body diode could be conducting at $t_2$ if the dead-time is overdimensioned.

[$t_2<t<t_3$, Fig. 9(c)]: at $t_2$, the switch $S_3$ turns on at the ZVS conditions and the converter enters the zero state, when the primary winding of the isolation transformer is shorted by the top transistors of the inverter bridge ($S_1$ and $S_3$). The voltage of the isolation transformer is zero and the magnetizing current remains unchanged at its maximum value (8).

[$t_3<t<t_4$, Fig. 9(d)]: at $t_3$, the current through the leakage inductance decreases to zero and the converter enters the discontinuous conduction mode (DCM). During DCM, the leakage inductance current remains zero and the power is not transferred from the input to the output side. Thanks to DCM, the VDR diodes feature ZCS, while the switch $S_1$ – near-ZCS.

[$t_4<t<t_5$, Fig. 9(e)]: at $t_4$, the switch $S_1$ turns off and the converter enters the dead-time interval. The current through the leakage inductance is still zero; therefore, the $S_1$ features near-ZCS combined with ZVS (due to magnetizing current) turn-off. The magnetizing current charges the output capacitance of $S_1$ while discharging the output capacitance of $S_2$. When the output capacitance of $S_2$ is fully discharged, its body diode starts conduction, which results in the ZVS turn on of the $S_2$ at the time instant $t_5$. Next, the converter enters the negative half-cycle, when the negative input voltage $V_{PV}$ is applied to the primary winding of the isolation transformer.

In the buck mode, the voltage stresses of the qZS capacitors are similar to those in the normal mode. The normalized voltage gain of the qZSSRC in the buck mode is similar to that of the traditional SRC with PSM control at the resonant frequency [23]:

$$G_{\text{buck(DCM)}} = \frac{V_{DC}}{2nV_{PV}} = 0.5 \cdot \left[ A \cdot \left( \frac{2}{\pi \cdot Q} - 1 \right) + \sqrt{\left( \frac{2}{\pi \cdot Q} - 1 \right)^2 A^2 + A \frac{8}{\pi \cdot Q}} \right] \tag{9}$$

where

$$A = 0.5 - 0.5 \cdot \cos \left[ \pi \cdot \left( 1 - \frac{\phi}{180} \right) \right] \tag{10}$$

$$Q = \frac{8 \cdot \pi \cdot f_{SW} \cdot L_{lk}}{R_L}. \tag{11}$$

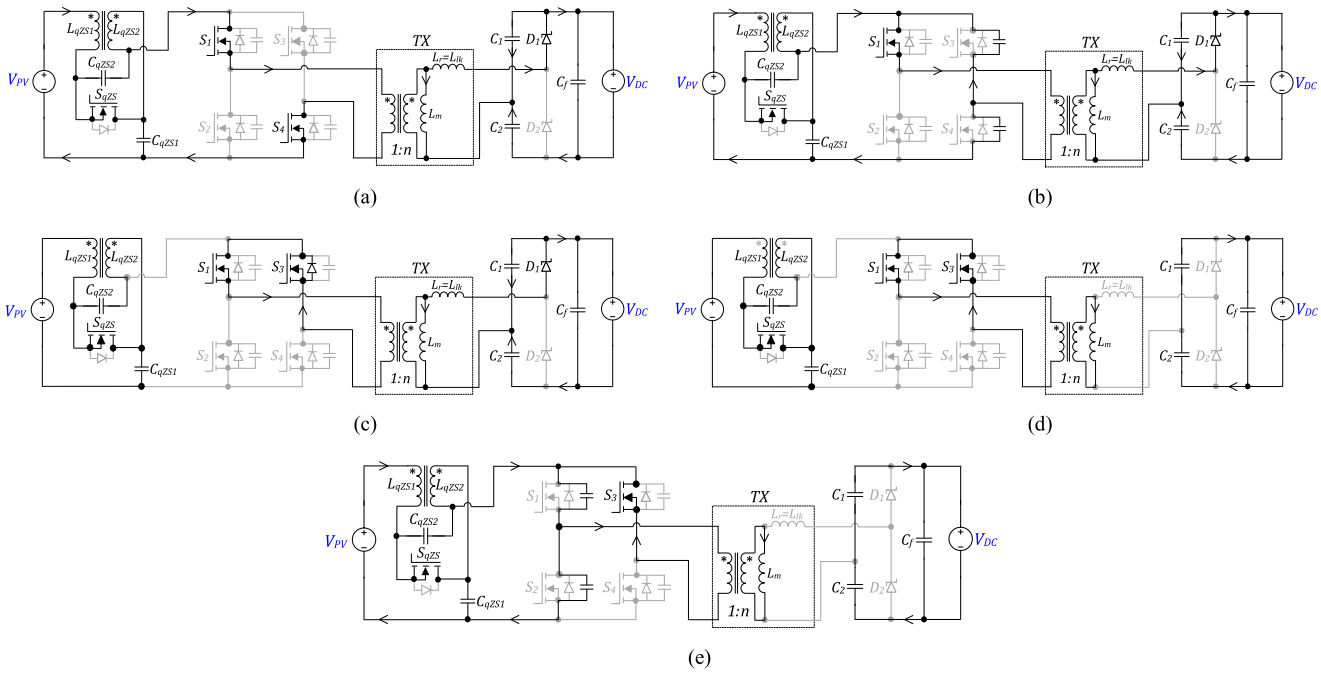


Fig. 9. Generalized equivalent circuits of the qZSSRC operating in the buck mode: (a) $t_0<t<t_1$, (b) $t_1<t<t_2$, (c) $t_2<t<t_3$, (d) $t_3<t<t_4$, and (e) $t_4<t<t_5$.

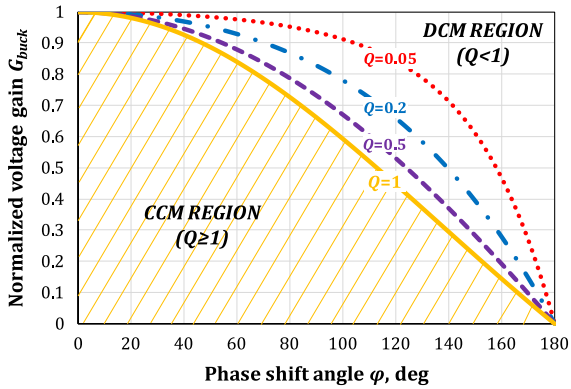


Fig. 10. Normalized voltage gain of the qZSSRC as a function of the phase-shift angle $\varphi$ for the different $Q$-factors of the resonant network.

Fig. 10 shows that the normalized voltage gain of the qZSSRC strongly depends on the $Q$-factor of the resonant tank and the phase-shift angle $\varphi$. It is important to notice that at $Q$-factors equal or higher than one, the converter starts operating with the continuous current through the resonant network and its regulation characteristic becomes more flat [24].

### C. Boost Mode

If the input voltage drops below the predefined nominal level, the converter starts to operate in the boost mode similar to the traditional qZS converter [20]. The output voltage is controlled by the PWM when the shoot-through states are generated by the symmetrical overlap of active states. Shoot-through states are generated by increasing the duty cycle of the switches over 0.5, which causes the active states of the top ($S_1$, $S_3$) and the bottom ($S_2$, $S_4$) switches to overlap each other [22]. The switching frequency of the qZSSRC in the boost mode remains fixed to the resonant frequency. In this case, the duration of the shoot-through state $t_{ST}$, i.e., when all the switches of the inverter bridge are simultaneously turned on, defines the dc voltage gain of the converter. The inverter switches are controlled without dead-time and the steady-state waveforms are shown in Fig. 11.

[$t_0<t<t_1$, Fig. 12(a)]: at $t_0$, all four switches of the inverter bridge are turned on and the converter enters the shoot-through state. The switch $S_{qZS}$ is turned off before the instant $t_0$ and its body diode is reverse-biased. The voltage stresses of the qZS capacitors could be estimated by

$$V_{CqZS1(\text{boost})} = \frac{V_{PV}(1-D_{ST})}{1-2D_{ST}};\ V_{CqZS2(\text{boost})} = \frac{V_{PV}D_{ST}}{1-2D_{ST}} \tag{12}$$

$$D_{ST} = \frac{t_{ST}}{T_{SW}}. \tag{13}$$

During the shoot-through state, the currents of the qZS inductor will linearly increase to their maximum value:

$$I_{LqZS(\max)} = I_{PV} + \frac{V_{PV}D_{ST}}{4L_{qZS}f_{SW}} \cdot \frac{1-D_{ST}}{1-2D_{ST}} \tag{14}$$

where $I_{PV}$ is the average input current of the converter and $L_{qZS}$ is the magnetizing inductance value of the qZS inductor.

[$t_1<t<t_2$, Fig. 12(b)]: at $t_1$, the switches $S_2$ and $S_3$ are turned off; the synchronous switch $S_{qZS}$ is turned on after dead-time and the active state begins. Diagonal switches $S_1$ and $S_4$ are conducting and the stepped-up voltage from the qZS network is applied to the primary winding of the isolation transformer

$$V_{TX,pr(\max)} = V_{CqZS1} + V_{CqZS2} = \frac{V_{PV}}{1-2D_{ST}}. \tag{15}$$

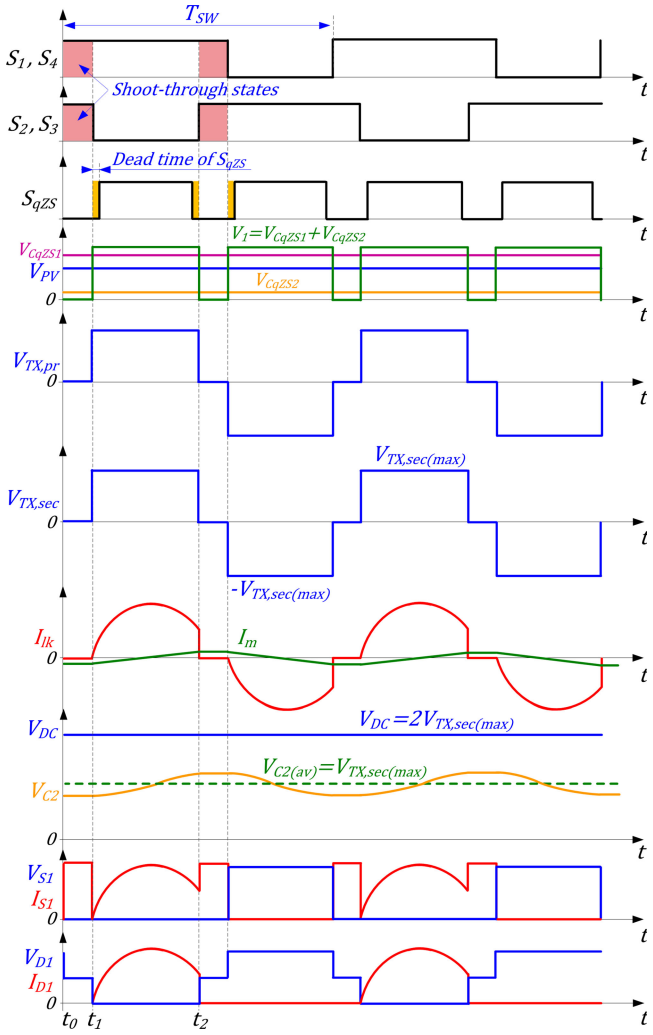


Fig. 11. Steady-state waveforms of the qZSSRC operating in the boost mode.

Similar to the normal mode, the current of the $L_{lk}$ and the voltage of parallel combination of $C_1$ and $C_2$ start resonating. The qZS inductor current is linearly decreasing to minimum

$$I_{LqZS(\min)} = I_{PV} - \frac{V_{PV} D_{ST}}{4 L_{qZS} f_{SW}} \cdot \frac{1 - D_{ST}}{1 - 2D_{ST}}. \tag{16}$$

At the instant $t_2$, the switches $S_2$ and $S_3$ are turned on, while the switch $S_{qZS}$ turns off before that instant. The resonance ends early and the converter enters the second shoot-though state similar to $[t_0<t<t_1]$. It is seen from Fig. 11 that in the boost mode, the inverter switches are always hard switched, while the VDR diodes feature the near-ZCS operation.

In order to prevent the damage of the circuit, which could be caused by the simultaneous conduction of the inverter transistors and synchronous switch $S_{qZS}$ during the shoot-through states, a dead-time is introduced before the turn on and off transients of the $S_{qZS}$, as shown in Fig. 11. During the dead-time, the body diode of the $S_{qZS}$ is conducting and the equivalent circuit of the converter during that time period is shown in Fig. 12(c). This state enables safe transition from the shoot-through to the active state and should be longer than the control signal propagation delay of the inverter switches.

The normalized voltage gain of the qZSSRC in the boost mode depends directly on the shoot-through duty cycle $D_{ST}$

$$G_{\text{boost}} = \frac{V_{DC}}{2\,nV_{PV}} = \frac{1}{(1 - 2D_{ST})}. \tag{17}$$

It is seen from Fig. 13 that for the threefold input voltage regulation range, the shoot-through duty cycle should vary in the range from 0 to 0.33. However, in real systems, the practical voltage gain in the boost mode could be seriously affected by the losses in the primary side of the converter where the major part is formed by the conduction losses of semiconductors [25].

## V. Converter Design and Control Considerations

### A. Magnetically Integrated qZS Network

To improve the power density, the proposed qZSSRC features the magnetically integrated qZS network, which is based on the coupled inductor with unity turns ratio. The highest current ripple through the coupled inductor occurs in the boost mode at the minimum input voltage, when the shoot-through duty cycle reaches its maximum value. Fig. 14 shows the equivalent circuit of the synchronous magnetically integrated qZS network.

Usually, the qZS network is considered symmetrical and, therefore, the leakage inductances are omitted from the design guidelines [26]. In real systems, the parasitic inductance of interconnection wires between the PV module and the converter ($L_w$) contributes to the input winding leakage inductance $L_{lk1}$, which results in different current ripples of the winding currents $I_1$ (i.e., $I_{PV}$) and $I_2$

$$\Delta I_1 = \frac{V_{ST(\min)} L_{lk1*} D_{ST(\max)} (1 - D_{ST(\max)})}{f_{SW}\,(L_{lk1*}L_{lk2} + L_{Mi}(L_{lk1*} + L_{lk2})) \cdot (1 - 2D_{ST(\max)})} \tag{18}$$

$$\Delta I_2 = \frac{V_{PV(\min)} L_{lk2} D_{ST(\max)} (1 - D_{ST(\max)})}{f_{SW}\,(L_{lk1*}L_{lk2} + L_{Mi}(L_{lk1*} + L_{lk2})) \cdot (1 - 2D_{ST(\max)})} \tag{19}$$

where $L_{lk1*}$ is the effective leakage inductance of the input winging of the coupled inductor ($L_{lk1*}=L_{lk1}+L_w$), $V_{PV(min)}$ is the minimum input voltage value of the converter, and $D_{ST(max)}$ is the corresponding maximum shoot-through duty cycle.

Generally, (18) and (19) are an extended version of (14) and (16), since they will provide the same results if leakage inductances are equal and converge to zero. Moreover, the current ripple ratio depends inversely proportional on the leakage inductances ratio, as shown in Fig. 15. However, the mismatch of the leakage inductance has only slight influence on the current of the magnetizing inductance $L_{Mi}$, as shown by the following expression (20) for the maximum magnetizing current

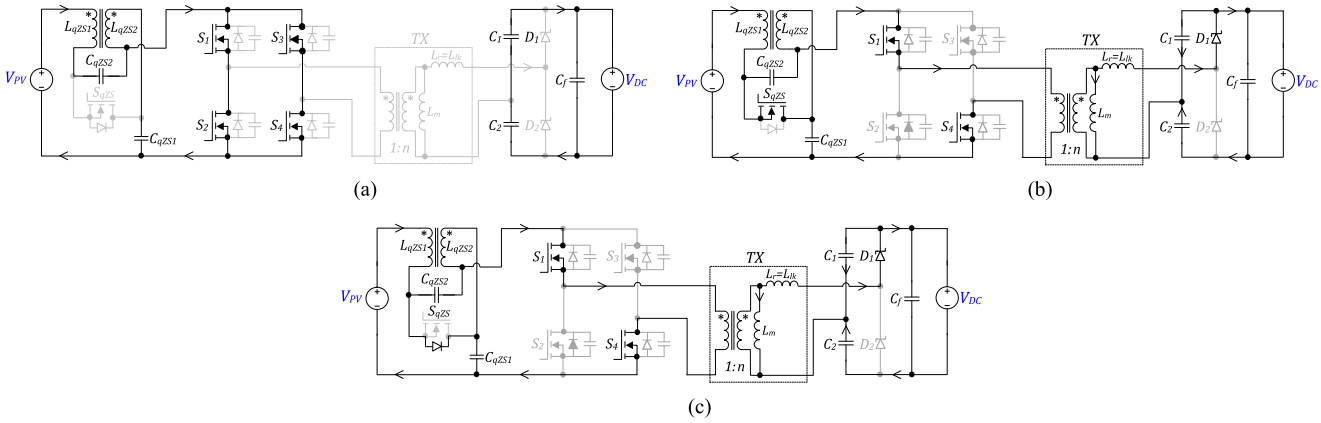


Fig. 12. Generalized equivalent circuits of the qZSSRC operating in the boost mode: (a) $t_0<t<t_1$, (b) $t_1<t<t_2$ and (c) during the dead-time of $S_{qZS}$.

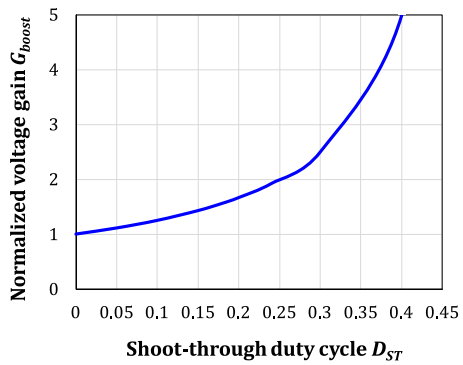


Fig. 13. Normalized voltage gain of the qZSSRC in the boost mode.

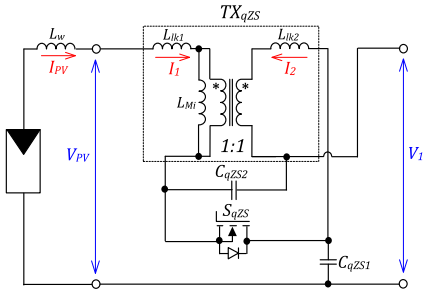


Fig. 14. Equivalent circuit of the magnetically integrated qZS network.

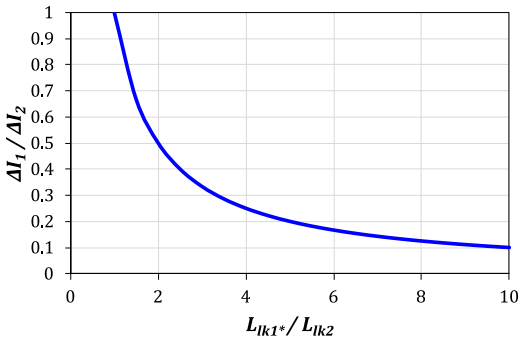


Fig. 15. Current ripple ratio as a function of the leakage inductance ratio.

$I_{LMi(\max)}$:

$$I_{LMi(\max)} = \frac{2P}{V_{PV(\min)}} + \frac{V_{PV(\min)} \cdot D_{ST(\max)} \cdot (1 - D_{ST(\max)})}{2 f_{SW} \left( \frac{L_{lk1*} \cdot L_{lk2}}{L_{lk1*} + L_{lk2}} + L_{Mi} \right) \cdot (1 - 2D_{ST(\max)})}. \quad (20)$$

Typically, the values of leakage inductances are considerably smaller than the magnetizing inductance value, even when considering parasitic inductance of interconnection wires. Hence, the simplified equation can be used for the dimensioning of the coupled inductor

$$I_{LMi(\max)} \approx \frac{2 \cdot P}{V_{PV(\min)}} + \frac{V_{PV(\min)} \cdot D_{ST(\max)} \cdot (1 - D_{ST(\max)})}{2 \cdot L_{Mi} \cdot f_{SW} \cdot (1 - 2D_{ST(\max)})}. \quad (21)$$

Due to the high current ripple in the qZS network, voltage ripple of the qZS capacitors ($\Delta V_{CqZS}$) has the highest value in the boost mode at the minimum input voltage

$$\Delta V_{CqZS} = \Delta V_{CqZS1} = \Delta V_{CqZS2} \approx \frac{P \cdot D_{ST(max)}}{C_{qZS} \cdot f_{SW} \cdot V_{PV(\min)}} \quad (22)$$

where $C_{qZS}$ is the capacitance of the qZS capacitors. It is evident that they feature the same absolute value of the voltage ripple, while their relative ripple is different. Average voltages of the qZS capacitors depend on the operating mode of the converter and can be found in Section III.

### B. Integrated Series Resonant Tank

To improve power density, the proposed converter contains a fully integrated series resonant tank at its secondary side (see Fig. 3), which is formed by the leakage inductance referred to the secondary winding ($L_{lk}$) of the isolation transformer and the parallel combination of the VDR capacitors ($C_1$+$C_2$). One of distinguishing features of the proposed converter is that due to the discontinuous current through the resonant network, it enables the ZCS of the inverter switches and VDR. Therefore, the critical value of the $L_{lk}$ when the converter still maintains

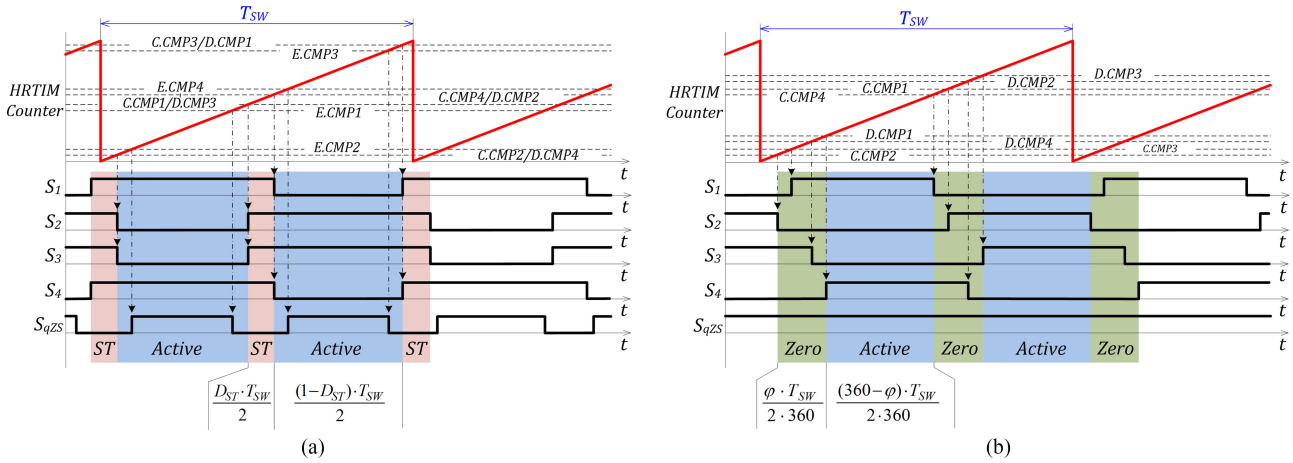


Fig. 16. Generalized principle of the control signal generation in (a) boost and (b) buck modes.

DCM could be found from (11) as follows:

$$L_{lk(\mathrm{cr,DCM})} < \frac{V_{DC}^2}{8\pi P f_{SW}}. \tag{23}$$

In high-frequency low-power transformers, the maximum value of the leakage inductance is significantly smaller than the critical value set by (23) since it is strictly limited by the physical design of the transformer. On the other hand, smaller values of $L_{lk}$ will lead to higher currents through the isolation transformer, which will result in increased current stresses of the semiconductors.

To maintain the resonance, the values of VDR capacitors could be selected by

$$C_1 = C_2 = \frac{1}{8L_{lk}\pi^2 f_{SW}^2}. \tag{24}$$

Since the discussed converter has its maximum efficiency in the normal mode, special attention should be paid to the proper selection of the dead-time. During the dead-time, the parasitic output capacitances of the inverter switches are charged and discharged by the magnetizing current of the transformer, which results in the robust full-ZVS and near-ZCS operation of the inverter switches. The minimal value of the dead-time could be found by

$$T_D \geq \frac{8L_m f_{SW} C_{\mathrm{oss}}}{n^2}. \tag{25}$$

where $C_{oss}$ is the parasitic output capacitance of the main switches.

### C. Multimode Control Principle

As described in Section III, the proposed converter features multimode operation to ensure the wide input voltage and load regulation. In the boost mode, the shoot-through PWM is used for the regulation of the output voltage. In the normal mode, the shoot-through states are eliminated and the converter operates as a typical voltage-fed SRC featuring fixed dc voltage gain. In the buck mode, the output voltage is controlled by the PSM at the resonant frequency. The carrier-based control signal generation of the proposed converter is shown in Fig. 16.

The control system requires a microcontroller, which utilizes the floating-point core or unit and enhanced PWM peripheral. It should contain high resolution timer (HRTIM) peripheral, which can generate at least ten PWM signals in order to achieve the maximum performance. Eventually, the HRTIM should be made of at least four 16-bit up-counters with synchronous auto-reload (further they are called units), while each of them should feature at least four compare registers. Clock frequency should be high enough in order to achieve acceptable PWM resolution to set short intervals, like dead-time, properly. For a converter with the switching frequency around 100 kHz, PWM clock frequency is recommended to be higher or equal to 200 MHz.

Control signals of switches $S_1$ and $S_2$ are controlled by the timer unit *C* and the corresponding compare values *C.CMP*1 . . . *C.CMP*4. Signals of switches $S_3$ and $S_4$ are controlled by the timer unit *D* and the corresponding compare values *D.CMP*1 . . . *D.CMP*4. Control signal of the synchronous switch $S_{qZS}$ is generated by the timer unit *E* and it is based on the compare values *E.CMP*1 . . . *E.CMP*4. All timer channels are synchronized and, therefore, only one counter sawtooth signal is shown in Fig. 16. Generally, every control signal requires only two compare values: one for setting it to logical "1" and the other for resetting to logical "0." However, the control signal of the $S_{qZS}$ has the double switching frequency as compared to other control signals. This means that it requires four compare values per switching period.

Calculation of the compare values is unified, since they are defined by the same equations in all operating modes. There is one main difference between the operating modes: in the boost mode, the phase-shift value $\varphi$ is equal to zero [see Fig. 16(a)], while the shoot-through duty cycle $D_{ST}$ is zero in the buck mode [see Fig. 16(b)]. Moreover, the synchronous switch $S_{qZS}$ is always turned on in the buck and normal modes. Hence, all the compare values of the timer unit *E* are ignored and its output is forced to the logical "1." Basically, the normal mode can be considered as the buck mode with zero phase shift. For simplicity of explanation, all compare values and the

TABLE II
EXPRESSIONS FOR CALCULATION OF THE COMPARE VALUES

| Comp. value | Expression | Comp. value | Expression |
|---|---|---|---|
| C.CMP1 | $0.5 + dt\_T - \frac{D_{ST}}{4}$ | D.CMP3 | $0.5 - \frac{\phi}{360} + dt\_T - \frac{D_{ST}}{4}$ |
| C.CMP2 | $\frac{D_{ST}}{4} - dt\_T$ | D.CMP4 | $1 - \frac{\phi}{360} + \frac{D_{ST}}{4} - dt\_T$ |
| C.CMP3 | $dt\_T - \frac{D_{ST}}{4}$ | E.CMP1 | $0.5 - \frac{D_{ST}}{4} - dt\_D\_off$ |
| C.CMP4 | $0.5 + \frac{D_{ST}}{4} - dt\_T$ | E.CMP2 | $0.5 + \frac{D_{ST}}{4} + dt\_D\_on$ |
| D.CMP1 | $1 - \frac{\phi}{360} + dt\_T - \frac{D_{ST}}{4}$ | E.CMP3 | $1 - \frac{D_{ST}}{4} - dt\_D\_off$ |
| D.CMP2 | $0.5 - \frac{\phi}{360} + \frac{D_{ST}}{4} - dt\_T$ | E.CMP4 | $\frac{D_{ST}}{4} + dt\_D\_on$ |

sawtooth signal are normalized to be within the range from 0 to 1, as shown in Fig. 16.

If the calculated compare value is higher than 1 or is negative, it has to be shifted to the next or the previous sawtooth period, correspondingly. Expressions for the calculation of the compare values are presented in Table II. They are taking into account the following relative dead-time values: *dt_T*—the qZS inverter transistors dead-time, *dt_D_on*—the transistor $S_{qZS}$ turn-on dead-time, and *dt_D_off*—the transistor $S_{qZS}$ turn-off dead-time.

## VI. EXPERIMENTAL VERIFICATION

### A. Description of the Prototype

For the experimental verification of the proposed concept, the prototype of the wide input voltage range PV microconverter based on the qZSSRC topology has been developed (see Fig. 18). General specifications of the prototype are listed in Table III.

The converter was designed to operate within the input voltage range from 10 to 60 V and with the power profile shown in Fig. 17. This power profile was specially synthesized to simulate the operation conditions of MLPE converters powered by the generic 60-, 72- and 80-cell PV modules with emphasis on the operation with 60-cell silicon PV modules due to their high market share [27]. It does not describe the behavior of any particular PV module, since no silicon PV module requires such wide voltage range. The power profile was designed as an integral assessment tool for galvanically isolated converters for PV MLPE applications, which provide an ultrawide input voltage range similar to that of nonisolated PV power optimizers.

The control system of the converter was realized on the ST STM32F334 microcontroller, which utilizes the Cortex-M4 core with a floating-point unit and enhanced PWM peripheral.

A simplified block diagram of the control system developed for the proposed converter is shown in Fig. 19. The input voltage sensor is nonisolated; however, the input current and output voltage sensors feature galvanic isolation. This architecture of the measurement subsystem results from the design of the control system that has common zero potential with the input side of the converter. Output signals of the sensors are then converted into a digital form using an integrated 12-bit analog-to-digital converter of the microcontroller.

TABLE III
GENERAL SPECIFICATIONS OF THE EXPERIMENTAL PROTOTYPE

| Operating parameters | |
|---|---|
| Input voltage range, $V_{PV}$ | 10–60 V |
| Nominal input voltage, $V_{PV,nom}$ | 34 V |
| Maximal input current, $I_{PV}$ | 12 A |
| Output voltage, $V_{DC}$ | 400 V |
| Switching frequency, $f_{SW}$ | 110 kHz |
| Dead-time of inverter switches | 120 ns |
| Dead-time of synchronous switch | 45 ns |
| Operating power range | 25–300 W |
| **Components** | |
| $S_1$–$S_4$, $S_{qZS}$ | Infineon BSC035N10NS5 |
| $D_1$, $D_2$ | CREE C3D02060E |
| $L_{qZS1}$, $L_{qZS2}$ | 22 µH |
| $C_{qZS1}$, $C_{qZS2}$ | 26.4 µF |
| $C_1$, $C_2$ | 43 nF |
| $C_f$ | 100 µF |
| $L_{lk}$ | 24 µH |
| $L_m$ | 1 mH |
| $n$ | 6 |

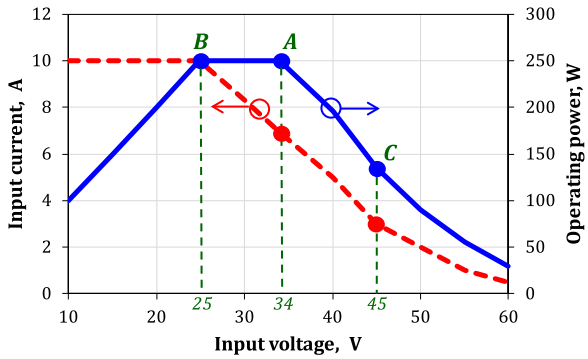


Fig. 17. Input current and operating power of the experimental prototype as functions of the input voltage.

Software control algorithm is executed only when the protection algorithm reports that the measured values are within the safety range. MPPT algorithm calculates the reference input voltage $V_{PV(ref)}$. Error between the reference and measured values of the input voltage is applied to the input of the PI controller. Saturation block with a mode selector allows smooth transition between the operating modes of the converter. Positive values of the PI controller output define the shoot-through duty cycle, while negative values determine the phase-shift angle. Shoot-through duty cycle and phase-shift angle define the compare values of the HRTIM, which is employed in the microcontroller. Equations for the calculation of the compare values are shown in Table II. The HRTIM generates control signals for the converter transistors. The physical output signals of the HRTIM are forwarded to the gate drivers of the corresponding transistors.

The proposed control system is quite simple since it does not control the dc-link voltage. In many distributed generation applications, the dc-link voltage is balanced by the power consumption of the load, i.e., inverter, energy storage, etc. Hence, the experimental study was performed by using the

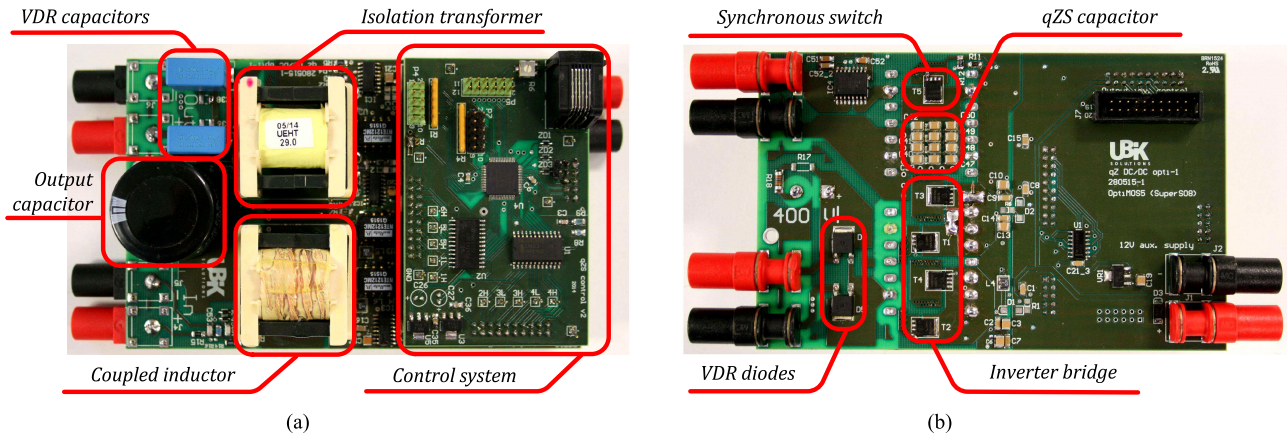


Fig. 18. (a) Top and (b) bottom views of the 300 W experimental prototype of the wide input voltage range PV microconverter based on the qZSSRC topology.

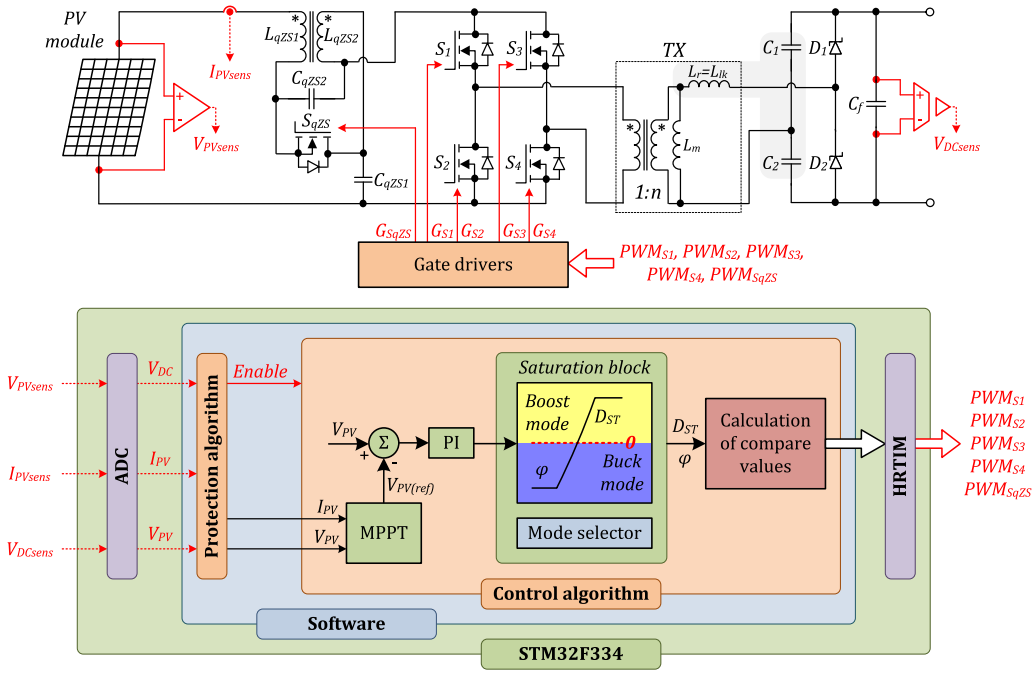


Fig. 19. Block diagram of the control system developed for the proposed converter.

electronic dc load in the constant voltage mode. If the dc-link voltage exceeds the limits defined for the normal operation, the protection algorithm will disable the converter operation.

### B. Experimental Results

Steady-state operating waveforms of the experimental multimode qZSSRC are presented in Figs. 20–22. To acquire the operating waveforms, the digital phosphor oscilloscope Tektronix DPO7254 equipped with the Rogowski coil current probe PEM CWTUM/015/R, current probe Tektronix TCP0030A, and high-voltage differential voltage probes Tektronix P5205A were used. The converter was supplied by the PV panel simulator Keysight E4360 and loaded by the programmable dc electronic load Chroma 63204.

First, the converter was tested in the normal mode at $V_{PV} = 34$ V and $P = 250$ W (point A in Fig. 17). The switching frequency was equal to the resonant frequency and the current through the isolation transformer has pure sinusoidal waveform [see Fig. 20(c)]. As a result, the inverter switches [see Fig. 20(d)] and VDR diodes [see Fig. 20(e)] are all operating under ZCS. Moreover, the inverter switches feature ZVS in addition to the near-ZCS due to magnetizing current recharging parasitic output capacitances. As can be seen from Fig. 20(c), the synchronous switch $S_{qZS}$ is constantly conducting, the voltage of capacitor $C_{qZS2}$ is zero, and the voltage of the capacitor $C_{qZS1}$ equals the input voltage.

Steady-state waveforms of the proposed converter in the buck mode with 45 V input and an operating power of 135 W are shown in Fig. 21 (point C in Fig. 17). To step-down the input voltage, the phase-shift angle between the two inverter legs was set to 130°. The operating waveforms [see Fig. 21(c)] reveal that the current through the isolation transformer is discontinuous.

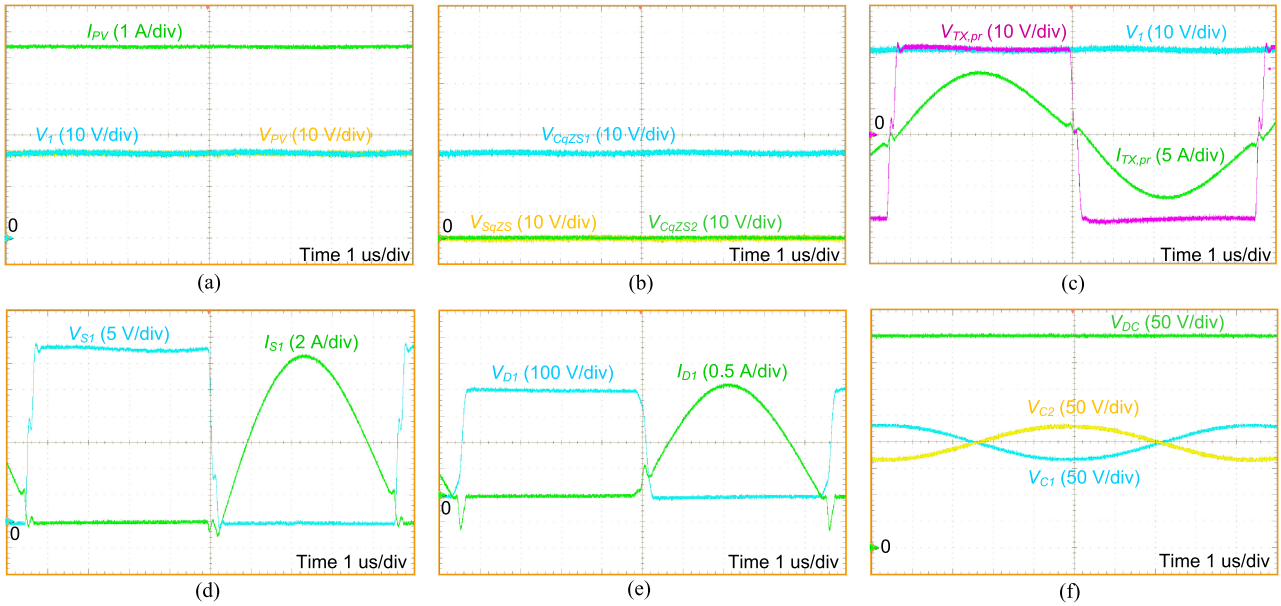


Fig. 20. Experimental waveforms of the qZSSRC in the normal mode at $V_{PV} = 34$ V and $P = 250$ W: (a) input voltage, input current, and intermediate dc-link voltage; (b) voltages of qZS capacitors and voltage of the switch $S_{qZS}$; (c) intermediate dc-link voltage and isolation transformer primary winding voltage and current; (d) voltage and current of switch $S_1$; (e) voltage and current of diode $D_1$; and (f) voltages of VDR capacitors and output voltage of the converter.

Hence, the VDR diodes are all operating under the full-ZCS [see Fig. 21(f)]. Inverter switches in the leading leg ($S_1$ and $S_2$) feature ZCS turn-on and near-ZCS combined with ZVS turn-off, which is supported by the magnetizing current of the isolation transformer. Switches in the lagging leg of the inverter are characterized by full-ZVS operation, which is ensured by the proper selection of the dead-time duration.

Finally, the converter was tested in the boost mode with 25 V input and an operating power of 250 W (point B in Fig. 17). To step-up the input voltage, the shoot-through duty cycle was set to 0.18. The experimental waveforms show that in the boost mode (see Fig. 22) the inverter MOSFETs are hard switched; however, the VDR diodes feature ZCS. Fig. 23 shows the experimentally obtained control variables of the proposed converter. It was confirmed that the converter is capable of ensuring the ripple-free 400 V output voltage within the sixfold input voltage variation (from 10 to 60 V). Moreover, due to influence of the input wires inductance, the converter features almost ripple-free continuous input current within the entire range of the input voltage and load variations.

Fig. 24 shows the efficiency curve of the experimental prototype, which was measured by the precision power analyzer Yokogawa WT1800. The efficiency curve incorporates all losses in the converter, including those of auxiliary power and the control system. As it was predicted, the peak efficiency (97.4 %) was achieved at the nominal input voltage when the converter operates in the normal mode and has the full soft-switching operation when near-ZCS and ZVS conditions are ensured. The efficiency drops to 87% in the boost mode when the converter operates at 100 W in the conditions of minimal input voltage and rated current ($V_{PV} = 10$ V, $I_{PV} = 10$ A). According to Fig. 23, the shoot-through duty cycle in this operating point has the maximum value of 0.41 and the converter demonstrates the maximum dc voltage gain of 40 ($G = V_{DC}/V_{PV}$ according to Fig. 1).

As it is seen from Fig. 17, the converter features maximum power in the voltage range from 25 to 34 V. Fig. 25 shows the efficiency curves as functions of the operating power acquired in the selected operating points within the maximum power range. The converter was also tested with the peak power of 300 W, which imposed no serious efficiency penalties. The peak efficiency obtained is within the target power range from 200 to 250 W.

As mentioned above, the proposed converter was specially designed for wide input voltage and load variations. According to the test profile presented in Fig. 17, the converter's operating power decreases gradually when the input voltage rises above 34 V. This operation range is mostly intended for the start-up of a PV module from the open-circuit voltage. Moreover, even at the nominal operating voltage ($V_{PV} = 34$ V) and at the part-load conditions ($P < 150$ W), the converter turns from the normal to the buck mode, which results in a remarkable efficiency drop (red line in Fig. 25). The operating mode was changed by the control system due to the tight stabilization of the output voltage at the level of $400 \pm 2$ V. The dc voltage gain and, consequently, the boundary between the operating modes depend slightly on the operating power. Therefore, the output voltage can reach values of up to 410 V at the input voltage of 34 V and under light-load conditions if the converter remains operating in the normal mode.

Remarkable efficiency drop at light-load requires modifications of the control algorithm, which will improve the part- and light-load efficiency. Among numerous available techniques, the cycle or pulse-skipping modulation is widely adopted in different applications, including PV systems [28]–[31]. The main idea is to force the converter into the idle mode when

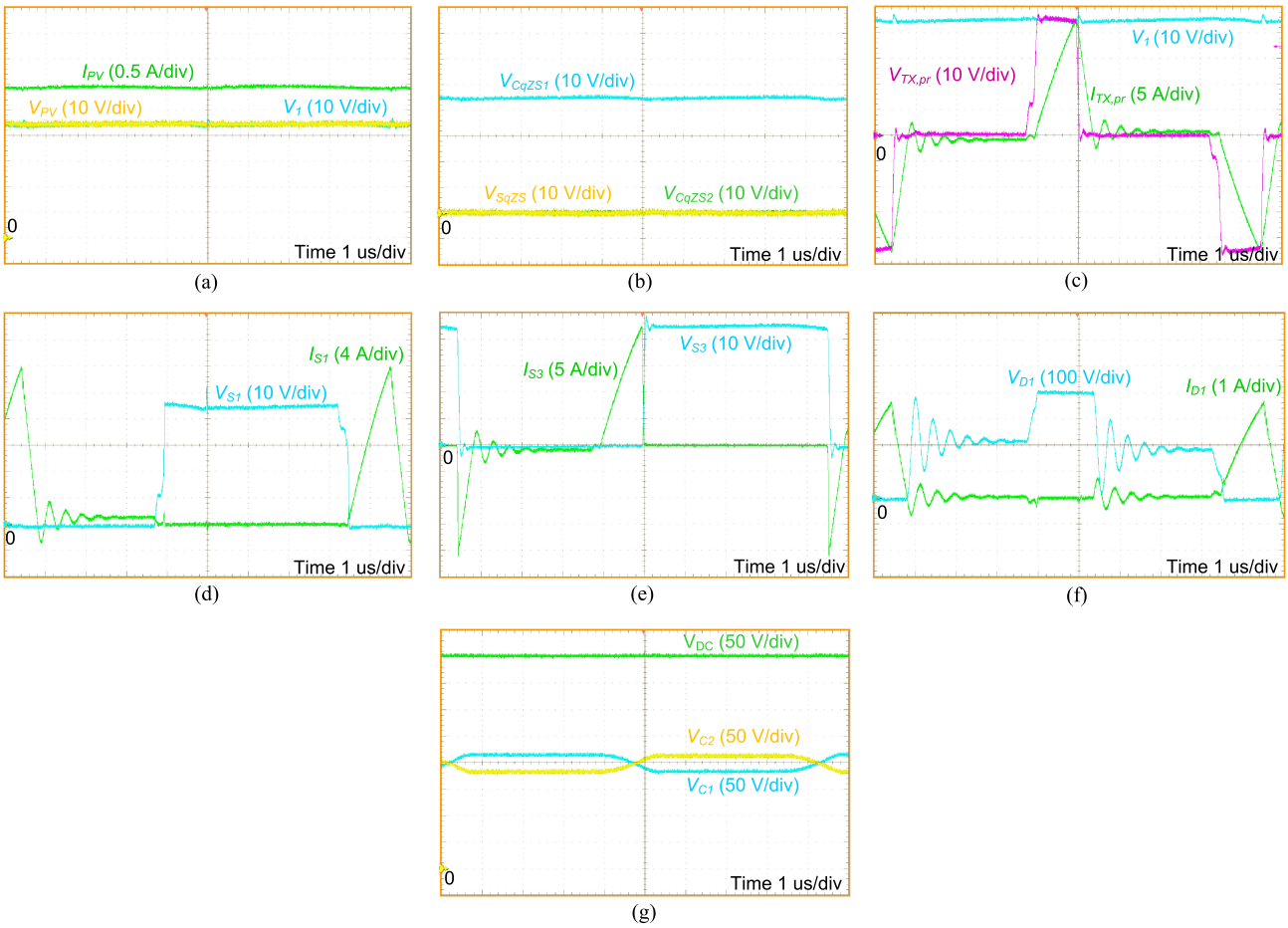


Fig. 21. Experimental waveforms of the qZSSRC in the buck mode at $V_{PV} = 45$ V, $P = 135$ W, and $\varphi = 130°$: (a) input voltage, input current, and intermediate dc-link voltage; (b) voltages of qZS capacitors and voltage of the switch $S_{qZS}$; (c) intermediate dc-link voltage and isolation transformer primary winding voltage and current, (d) voltage and current of switch $S_1$; (e) voltage and current of switch $S_3$; (f) voltage and current of diode $D_1$; and (g) voltages of VDR capacitors and output voltage of the converter.

all switches are turned off, for several switching periods after one switching period of normal operation. Efficiency for the boost and the normal modes was measured above in different operating points. However, it is evident from Fig. 24 that the converter suffers most from the efficiency drop in the buck mode. It should be noted that the efficiency in that mode was not studied comprehensively. Therefore, the buck mode was selected to analyze the cycle-skipping modulation for clear illustration of its benefits. It was compared with the normal mode below.

The experimental study was performed for two operating points: $V_{PV} = 34$ V and $V_{PV} = 45$ V. In the first case, the converter turns from the normal mode to the buck mode when the operating power decreases below 150 W. In the second case, the converter is in the buck mode at any operating power. Efficiency improvement resulted from the application of the cycle-skipping modulation is shown in Fig. 26. In the figure, different modulations are designated as $1/Y$, where $Y$ is the number of skipped switching periods, when the converter is in the idle mode. It means that 1/0 corresponds to modulation without cycle skipping, while 1/5 corresponds to modulation that skips five switching periods after a single switching period of the operation. This results in decreased switching and magnetic losses at part- and light-load operation. However, at switching frequencies of around 100 kHz, skipping of more than five cycles is not recommended in order to avoid audible frequency range.

It is apparent from Fig. 26 that for each input voltage value, it is possible to draw an envelope over the efficiency curves with an efficiency variation of roughly 1% within the operating power variation range of 25–150 W. At $V_{PV} = 34$V, points on the envelope correspond to the pure normal mode with skipping of one, two or three cycles depending on the instantaneous operating power, while other points employ PSM with a small phase-shift angle. Operation in the normal mode at all power levels results in an efficiency improvement of up to 4%, while maintaining the output voltage of $400\,\text{V} \pm 1\%$. In the second case, the envelope of efficiency curves corresponds to PSM with skipping of two cycles in the range of the operating power of 75–150 W, while at the lower operating powers, the PSM with skipping of five cycles has to be adopted. This enables an efficiency improvement roughly by 10% at the minimum operating power.

To achieve part- and light-load efficiency improvement over the entire operating range of the converter, a similar

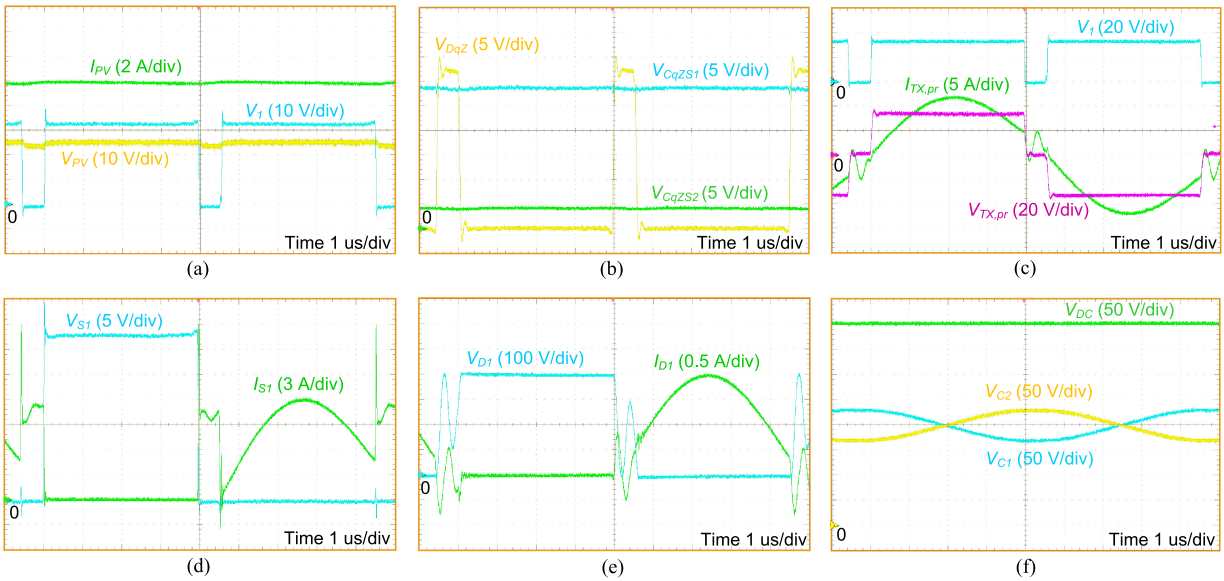


Fig. 22. Experimental waveforms of the qZSSRC in the boost mode at $V_{PV} = 25\,\text{V}$, $P = 250\,\text{W}$, and $D_S = 0.18$: (a) input voltage, input current, and intermediate dc-link voltage, (b) voltages of qZS capacitors and voltage of the switch $S_{qZS}$, (c) intermediate dc-link voltage and isolation transformer primary winding voltage and current, (d) voltage and current of switch $S_1$, (e) voltage and current of diode $D_1$, and (f) voltages of VDR capacitors and output voltage of the converter.

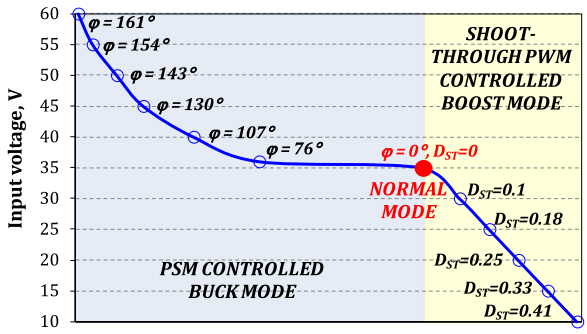


Fig. 23. Experimental control variables of the proposed converter.

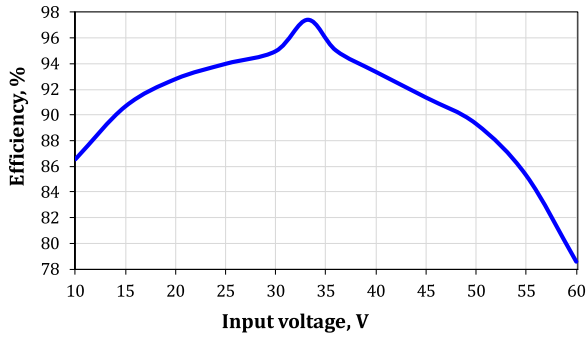


Fig. 24. Experimental efficiency of the proposed converter measured according to the power profile from Fig. 17.

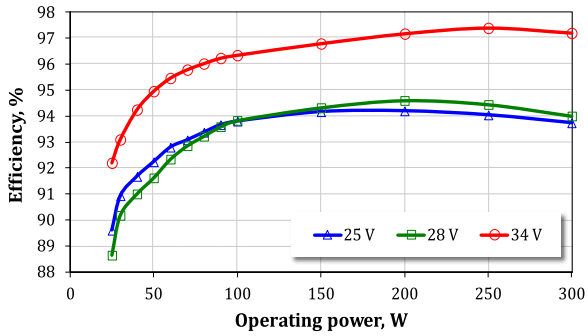


Fig. 25. Experimental efficiency of the proposed converter in the MPP range.

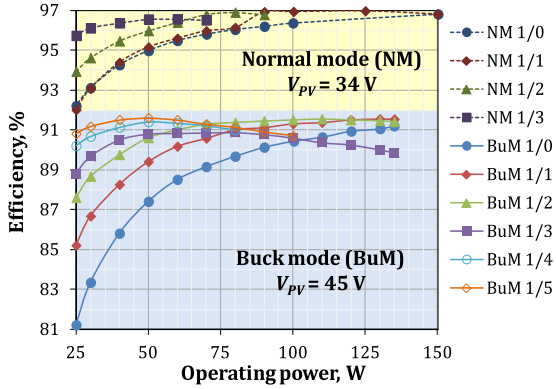


Fig. 26. Part- and light-load efficiency improvement of the proposed converter by the use of the cycle-skipping technique.

experimental study is required for the rest of the operating points. It will result in a map of an optimal number of skipped cycles for each possible operating point, which, in turn, will help to achieve a more flat efficiency curve of the converter. The main disadvantage of the cycle skipping modulation is in the increased input current ripple that usually results in deteriorated MPPT performance [32]. The converter, i.e., passive components of the qZS network, should be designed for the lowest possible switching frequency to improve the energy harvest under the light-load conditions when the cycle skipping modulation is adopted. Otherwise, the efficiency rise from the

cycle-skipping modulation will not result in improved energy yield.

## VII. Conclusion

This paper has introduced a novel single-stage galvanically isolated high step-up dc–dc converter for the PV MLPE applications. Thanks to the multimode operation, the proposed qZSSRC with synchronous qZS network and series resonant tank integrated to the secondary part of the converter features a wide input voltage and load regulation range. Moreover, the proposed topology achieves high efficiency through the full-ZCS of the VDR diodes over the entire operating range, and depending on the operating mode, ZVS and/or ZCS of the primary-side switches.

The multimode operation principle of the proposed converter was described along with steady-state waveforms and analysis of operating states. Next, selected design guidelines were presented for the integrated magnetic components and realization of the control system. To verify the theoretical assumptions, the experimental prototype was assembled and tested. It was confirmed that the proposed converter is capable of ensuring the ripple-free 400 V output voltage within the sixfold variation of the input voltage (from 10 to 60 V). Moreover, it features the continuous input current over the entire voltage and load variation range without adding the buffering capacitors to its input terminals. The converter prototype based on the generic Si MOSFETs and SiC SBDs achieves the maximum efficiency of 97.4% in the nominal mode and at the rated power of 250 W. It was also shown how the part- and light-load efficiency of the proposed converter can be improved considerably by the use of the cycle-skipping modulation technique.

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